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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/699,390 | 10/31/2003 | Yung-Hung Chen | 250606-1010 | 3274 |

24504 7590 05/11/2005

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| EXAMINER | |
|---|---|
| TRA, ANH QUAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,390 | CHEN, YUNG-HUNG | |
| | Examiner | Art Unit | |
| | Quan Tra | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-14* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the amendment filed 12/10/04. The rejection in previous office action is maintained.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5, 8, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim (USP 67778007).

As to claim 1, Lim discloses in figure 7 a voltage reference generator for generating an output voltage (VINT) at an output node, comprising: a level shifter (P4, P3) for s shifting a first reference voltage (voltage at the gate of P4) into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and a feedback circuit (10) for monitoring the output voltage and a second reference voltage (VREF) to control the shift and to normalize the output and second reference voltages.

As to claim 2, figure 7 shows that the level shifter includes a source follower (P4) coupled between a voltage source (ground) and the output node, the source follower having an input node (gate) for receiving the first reference voltage.

As to claim 3, figure 7 shows that the source follower has an MOS transistor having a drain connected to the voltage source, a source as the output node and a gate at the input node,

and further having a current source (P3) controlled by the feedback circuit and connected to the source of the MOS transistor.

As to claim 5, figure 7 MOS transistor is a PMOS transistor.

As to claim 8, figure 10 shows that the MOS transistor is a NMOS transistor.

As to claim 12, figure 7 shows that the feedback circuit has a differential amplifier with an inverted input, a non-inverted input and an output, the non-inverted input coupled to the output node, the inverted input coupled to the second reference voltage, and the output coupled to a current source (P3) in the level shifter to control the shift of the level.

As to claim 14, figure 7 shows a voltage divider (R4, R6) to provide the first reference voltage (at the gate of P4) and a third reference voltage (voltage at one of the connection nodes of resistors R7 in figures 9A and B).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 6, 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (USP 67778007) in view of Khalid (US 20040150464) (previously cited).

As to claim 4, Lim's figure 7 shows all limitations of the claim except for the MOS transistor is a NMOS transistor. However, Khalid's figures 1A and 1B show that reversing the type of transistors and the polarity in a voltage generation is well known. Therefore, it would have been obvious to one having ordinary skill in the art to reverse the structure of Lim's figure

7 by reversing the transistor types and the power supplies in order to take advantage of the benefit of Lim's circuit and use the circuit a different environment that requires a reverse type power supply circuit. Thus, the modified Lim's figure 7 shows the MOS transistor is NMOS transistor.

As to claim 6, the modified Lim's figure 7 shows that the current source (P3) (P3 now is an NMOS transistor) is an MOS transistor having a drain connected to the output node, a source connected to a ground, and a gate connected to the output of the differential amplifier.

As to claim 7, the modified Lim's figure 7 shows a constant current source (IL) coupled between the output node and another voltage source.

As to claim 13, Lim's figure 10 shows all limitations of the claim except for a low-pass filter connected between output of the differential amplifier and current source in the level shifter. However, Khalid's figure 1B shows a low-pass filter 12 coupled to the output of differential amplifier 11 and to the gate of current source 13 in order to filter the output voltage of the amplifier 11. Therefore, it would have been obvious to one having ordinary skill in the art to add a low-pass filter to the output of Lim's differential amplifier for the purpose of filtering the output of the amplifier.

***Allowable Subject Matter***

5. Claims 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10 and 11 would be allowable because the prior art fails to teach or suggest a low-pass filter to filter out a high frequency portion of the first reference voltage and direct the first reference voltage to the level shifter.

***Response to Arguments***

6. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that P4 is not a level shifter. The Examiner respectfully disagrees. As broadest reasonable interpretation, level shifter is a circuit that generating an output voltage that has a level different from its input voltage level. One skill in the art would have realized that the input and output of P4 have different voltage levels. Thus, P4 is a level shifter.

Applicant argues that there is no motivation to combine the teachings of Lim and Khalid. The examiner respectfully disagrees. Khalid's figure 1 shows that reversing the polarity and transistor types in a voltage generation circuit is well known. One skill in the art would have motivated to reverse the polarity and transistor types in Lim in order to take the advantage of the benefit of Lim's voltage generation and use the modified voltage generation circuit in a different environment that required such advantage.

Further, It is not necessary that the cited references or prior art actually suggest expressly or in so many words, the changes or improvements that applicant has made. The test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. In re Sheckier, 168 USPQ 716 (CCPA 1971): In re McLaughlin 170 I USPQ 209 (CCPA 1971); In re Young 159 USPQ 725 (CCPA 1968).

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

May 9, 2005